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REMARKS

Claims 1-29 are pending in the application. Favorable reconsideration of the application is respectfully requested.

I. *REJECTION OF CLAIMS 1-4 UNDER 35 USC §102(e)*

Claims 1-4 stand rejected under 35 USC §102(e) based on *Ito*. This rejection is respectfully traversed for at least the following reasons.

Claim 1 describes a controller for controlling the frame refresh rate of an active matrix display in accordance with the present invention. The controller includes a first circuit responsive to display signals from a display controller *for supplying an enable signal (FE) for each Nth frame, where N is an integer greater than zero and is selectable from a plurality of values*. In addition, the controller includes a second circuit for enabling refreshing of the display by each Nth frame supplied to the display controller in response to the enable signal (FE). Moreover, the second circuit *prevents refreshing of the display by each other frame* supplied to the display controller in the absence of the enable signal (FE).

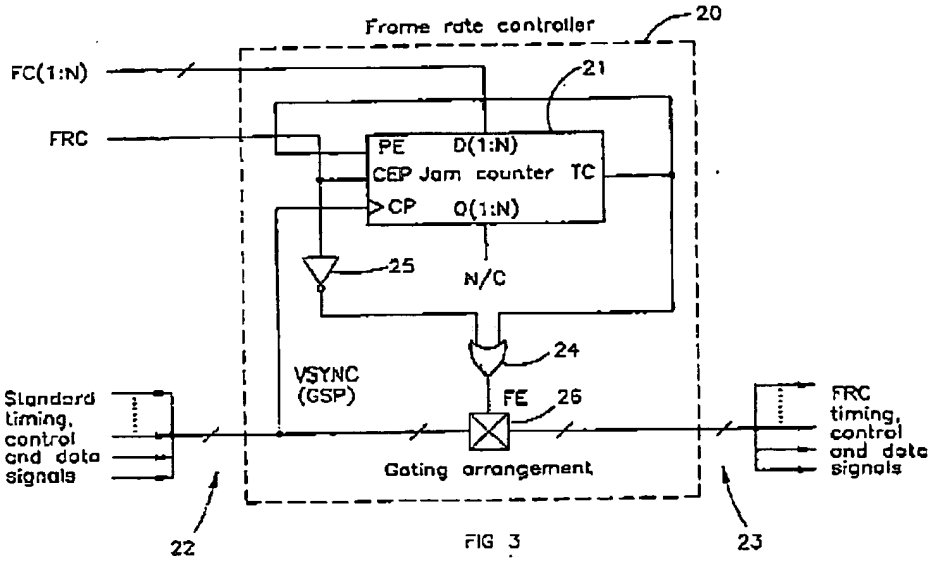

Fig. 3 of Present Application

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Fig. 3 of the present application (reproduced above) illustrates, for example, how a controller 20 accepts a value FC which controls a counter 21 incremented with each vertical sync pulse (VSP). The output of the counter 21 is used to form an enable signal FE coupled to a gating arrangement 26.

As a result, the controller 20 enables the refreshing of the display each nth frame supplied to the display controller as recited in claim 1. Moreover, the controller 20 prevents refreshing of the display by each other frame supplied to the display controller in the absence of the enable signal FE as further recited in claim 1. The value of FC is selectable among a plurality of values and can be any integer value greater than zero.

The present application describes how such features may be advantageous in reducing power consumption, for example. Specifically, by controlling the frame refresh rate the power consumption can be reduced. Moreover, the present invention allows it to be done via a simple circuit arrangement. (See, e.g., Spec., p. 31, ln. 12 to p. 32, ln. 8).

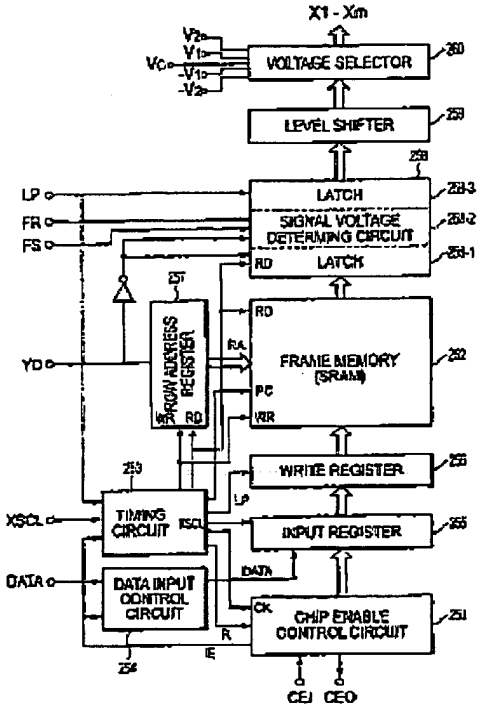

Fig. 11 of Ito

The Examiner relies on Fig. 11 of *Ito* (reproduced above) as teaching a controller as recited in claim 1. Applicants must respectfully disagree.

Specifically, the Examiner refers to a chip enable control circuit 251 which provides an enable signal E. The Examiner further refers to the row address register 257 as enabling the refreshing of the display.

Applicants respectfully submit that the circuit in Fig. 11 of *Ito* has very little to do with the frame refresh rate controller recited in claim 1. More particularly, Fig. 11 of *Ito* discloses a signal electrode driving circuit for providing the signal line voltages to a display. *Ito* does describe the chip enable control circuit 251 as providing an automatic power saving circuit. However, *Ito* does not include any teaching or suggestion of the chip enable control circuit 251 supplying an enable signal for each Nth frame of data as recited in claim 1.

For example, applicants note that the frame start pulse YD (arguably analogous to a vertical sync pulse used to identify frames in the exemplary embodiment of the present invention) is *not* provided to the chip enable control circuit 251. Therefore, the chip enable control circuit 251 is by no means serving as a counter to determine every Nth frame, for example. There is simply no teaching or suggestion in *Ito* as to how the chip enable control circuit 251 may be responsive to signals from a display controller for supplying an enable signal for each Nth frame, where N is an integer greater than zero and is selectable from a plurality of values. The Examiner's reliance on Figs. 2 and 6 of *Ito* is misplaced as although the figures illustrate multiple frames, there is no teaching or suggestion of an enable signal being supplied as recited in claim 1.

Furthermore, the row address register 257 is conventional in sequentially selecting a row (word line) of the frame memory 252. Again, *Ito* does not include any teaching or suggestion of controlling the refreshing of the display by each Nth frame while preventing the refreshing of the display by each of the other frames supplied to the display controller as recited in claim 1.

The Examiner refers to Col. 17, lines 54-66 of *Ito* as purportedly teaching the enabling refreshing of the display by each Nth frame, where N is greater than zero and selectable from a plurality of values. Applicants respectfully disagree. *Ito* admittedly

refers to the chip enable circuit 25 serving as an automatic power saving circuit responsive to an active low signal. However, there is no teaching or suggestion that such an active low signal is in any way representative of or leads to a result of an enable signal for each Nth frame, where N is an integer greater than zero and is selectable from a plurality of values as recited in claim 1.

For at least the above reasons, applicants respectfully submit that *Ito* does not teach or suggest each and every element recited in claim 1. Withdrawal of the rejection of claim 1 and the claims which depend therefrom is respectfully requested.

II. REJECTION OF CLAIMS 5-29 UNDER 35 USC §103(a)

Claims 5-29 stand rejected under 35 USC §103(a) based on *Ito* in view of *Ohara et al.* This rejection is respectfully traversed for at least the following reasons.

Claims 5-29 each depend from claim 1 either directly or indirectly. Therefore, these claims may be distinguished over the teachings of *Ito* for at least the same reasons discussed above in relation to claim 1. Furthermore, *Ohara et al.* does not make up for the above-discussed deficiencies in *Ito*.

As a result, withdrawal of the rejection is respectfully requested.

III. CONCLUSION

Accordingly, all claims 1-29 are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

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Should a petition for an extension of time be necessary for the timely reply to the outstanding Office Action (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

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